Intermediate Frequency Receiver, 800 MHz to 4000 MHz

Data Sheet

HMC8100LP6JE

FEATURES

High linearity: supports modulations to 1024 QAM
Rx IF range: 80 MHz to 200 MHz
Rx RF range: 800 MHz to 4000 MHz
Rx power control: 80 dB
SPI programmable bandpass filters
SPI controlled interface
40-lead, 6 mm × 6 mm LFCSP package

APPLICATIONS

Point to point communications
Satellite communications
Wireless microwave backhaul systems

GENERAL DESCRIPTION

The HMC8100LP6JE is a highly integrated intermediate frequency (IF) receiver chip that converts radio frequency (RF) input signals ranging from 800 MHz to 4000 MHz down to a single-ended intermediate frequency (IF) signal of 140 MHz at its output.

The IF receiver chip is housed in a compact 6 mm × 6 mm LFCSP package and supports complex modulations up to 1024 QAM. The HMC8100LP6JE device includes two variable gain amplifiers (VGAs), three power detectors, a programmable automatic gain control (AGC) block, and selected integrated band-pass filters with 14 MHz, 28 MHz, 56 MHz, and 112 MHz bandwidth. The HMC8100LP6JE also supports baseband IQ interfaces after the mixer so that the chips can be used in the full outdoor units (ODU) configuration. The HMC8100LP6JE supports all standard microwave frequency bands from 6 GHz to 42 GHz.

FUNCTIONAL BLOCK DIAGRAM

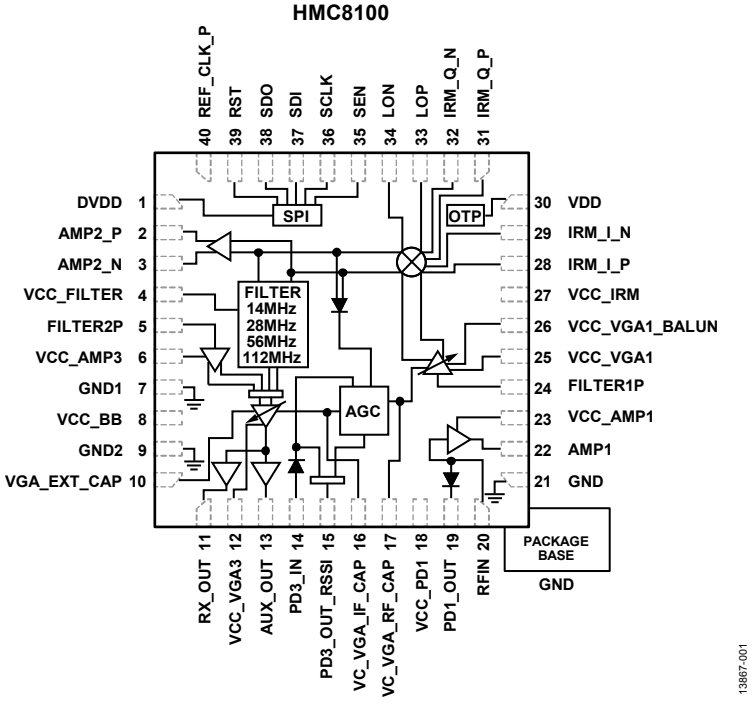

Figure 1.

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9/2017—Rev. A to Reb. B

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5/2016—v00.0416 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.
Updated Format ..... Universal
Added Pin Configuration Diagram, Renumbered Sequentially 7
Added Ordering Guide 22

04/2016—v00.0416: Initial Version

SPECIFICATIONS

T_A = 25°C, IF frequency = 140 MHz, local oscillator (LO) input signal level = 0 dBm, RF input signal level = −80 dBm per tone, filter bandwidth = 56 MHz, IF gain limit (decimal) = 7, sideband select = lower sideband, AGC select = external AGC, unless otherwise noted, see the Typical Performance Characteristics section.

ELECTRICAL CHARACTERISTICS: 800 MHz TO 1800 MHz RF FREQUENCY RANGE

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
LO Frequency Range	600		2000	MHz
IF Frequency Range	80		200	MHz
RF INPUT INTERFACE				
Input Impedance		50		Ω
Return Loss		10		dB
IF OUTPUT INTERFACE				
Input Impedance		50		Ω
Return Loss	8	13		dB
LO INPUT INTERFACE				
Input Impedance		50		Ω
Return Loss	2	9		dB
DYNAMIC PERFORMANCE				
Power Conversion Gain	81	86		dB
RF VGA Dynamic Range	40	52		dB
IF VGA Dynamic Range		49		dB
Image Rejection	30	36		dBc
Noise Figure at P_{IN} (One Tone)		5	8	dB
Output Third-Order Intercept (OIP3)	11	16		dBm
Output 1 dB Compression Point (OP1dB)	7	11		dBm
LO Leakage at the IF Input		−48	−26	dBm
LO Leakage at the RF Input		−75	−70	dBm
RF Leakage at the IF Output		−68	−60	dBm
POWER SUPPLY				
Supply Voltage				
V_{CCX}		3.3		V
V_{CC} – VGA[1]		3.3		V
Supply Current				
V_{CCX}		600		mA
V_{CC} – VGA[1]		11		µA

[1] V_{CC} – VGA = VC_VGA_IF + VC_VGA_RF can be adjusted from 3.3 V (minimum ATTEN) to 0 V (maximum ATTEN) to control the IF and RF VGA in external AGC mode.

ELECTRICAL CHARACTERISTICS: 1800 MHz TO 2800 MHz RF FREQUENCY RANGE

Table 2.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
LO Frequency Range	1600		3000	MHz
IF Frequency Range	80		200	MHz
RF INPUT INTERFACE				
Input Impedance		50		Ω
Return Loss		12		dB
IF OUTPUT INTERFACE				
Input Impedance		50		Ω
Return Loss	8	13		dB
LO INPUT INTERFACE				
Input Impedance		50		Ω
Return Loss	7	15		dB
DYNAMIC PERFORMANCE				
Power Conversion Gain	77	85		dB
RF VGA Dynamic Range	40	47		dB
IF VGA Dynamic Range	40	49		dB
Image Rejection	30	36		dBc
Noise Figure at P_{IN} (One Tone)		5	7	dB
Output Third-Order Intercept (OIP3)	11	18		dBm
Output 1 dB Compression Point (OP1dB)	7	11		dBm
LO Leakage at the IF Input		−55	−45	dBm
LO Leakage at the RF Input		−73	−66	dBm
RF Leakage at the IF Output		−73	−65	dBm
POWER SUPPLY				
Supply Voltage				
V_{CCX}		3.3		V
V_{CC} – VGA[1]		3.3		V
Supply Current				
V_{CCX}		600		mA
V_{CC} – VGA[1]		11		µA

[1] V_{CC} – VGA = VC_VGA_IF + VC_VGA_RF can be adjusted from 3.3 V (minimum ATTEN) to 0 V (maximum ATTEN) to control the IF and RF VGA in external AGC mode.

ELECTRICAL CHARACTERISTICS: 2800 MHz TO 4000 MHz RF FREQUENCY RANGE

Table 3.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
LO Frequency Range	2600		4200	MHz
IF Frequency Range	80		200	MHz
RF INPUT INTERFACE				
Input Impedance		50		Ω
Return Loss		13		dB
IF OUTPUT INTERFACE				
Input Impedance		50		Ω
Return Loss	8	13		dB
LO INPUT INTERFACE				
Input Impedance		50		Ω
Return Loss	7	14		dB
DYNAMIC PERFORMANCE				
Power Conversion Gain	72	82		dB
RF VGA Dynamic Range	35	47		dB
IF VGA Dynamic Range		49		dB
Image Rejection	30	38		dBc
Noise Figure at P_{IN} (One Tone)		5	8	dB
Output Third-Order Intercept (OIP3)	12	22		dBm
Output 1 dB Compression Point (OP1dB)	7	12		dBm
LO Leakage at the IF Input		−65	−48	dBm
LO Leakage at the RF Input		−66	−62	dBm
RF Leakage at the IF Output		−72	−65	dBm
POWER SUPPLY				
Supply Voltage				
V_{CCX}		3.3		V
V_{CC} – VGA[1]		3.3		V
Supply Current				
V_{CCX}		600		mA
V_{CC} – VGA[1]		11		µA

[1] V_{CC} – VGA = VC_VGA_IF + VC_VGA_RF can be adjusted from 3.3 V (minimum ATTEN) to 0 V (maximum ATTEN) to control the IF and RF VGA in external AGC mode.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
RF Input	10 dBm
LO Input	10 dBm
VCCX	−0.5 V to +5.5 V
	−0.3 V to +3.6 V
Maximum Junction Temperature to Maintain 1 Million Hour MTTF	150°C
Thermal Resistance (RTH), Junction to Ground Paddle	10.5°C/W
Temperature	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
Maximum Peak Reflow Temperature (MSL3)	260°C
ESD Sensitivity (Human Body Model)	2000 V (Class 2)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

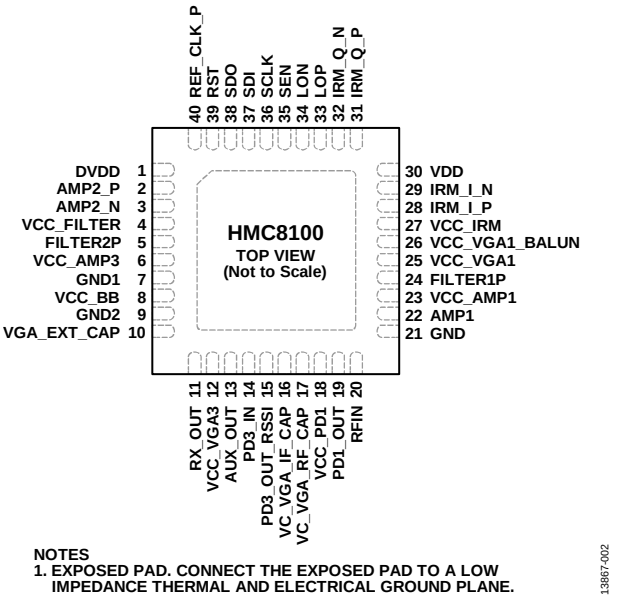


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DVDD	SPI Digital Power Supply (3.3 V dc). See Figure 52 for the required components.
2	AMPT2_P	Second Differential Amplifier Output (Positive).
3	AMP2_N	Second Differential Amplifier Output (Negative).
4	VCC_FILTER	Power Supply for the Filter (3.3 V dc). See Figure 52 for the required components.
5	FILTER2P	Input of the Third External Filter Amplifier.
6	VCC_AMP3	Power Supply for the Third External Filter Amplifier (3.3 V dc). See Figure 52 for the required components.
7, 9, 21	GND1, GND2, GND3	Ground Connect.
8	VCC_BB	Power Supply for the Baseband Blocks (3.3 V dc). See Figure 52 for the required components.
10	VGA_EXT_CAP	External Capacitor for VGA3. See Figure 52 for the required components.
11	RX_OUT	Receiver Output.
12	VCC_VGA3	Power Supply for VGA3 (3.3 V dc). See Figure 52 for the required components.
13	AUX_OUT	Receiver Auxiliary Output.
14	PD3_IN	Receive AGC Loop Input.
15	PD3_OUT/RSSI	Third Power Detector Output.
16	VC_VGA_IF/CAP–	Control Voltage of IFVGA/AGC Integrator Capacitor. See Figure 52 for the required components.
17	VC_VGA_RF/CAP+	Control Voltage of RFVGA/AGC Integrator Capacitor. See Figure 52 for the required components.
18	VCC_PD1	Power Supply for the First Power Detector (3.3 V dc). See Figure 52 for the required components.
19	PD1_OUT	First Power Detector Output.
20	RFIN	Radio Frequency Input. This pin is matched to 50 Ω.
22	AMP1	Single-Ended Output of Amplifier 1 (3.3 V dc). See Figure 52 for the required components.
23	VCC_AMP1	Power Supply for AMP1 (3.3 V dc). See Figure 52 for the required components.
24	FILTER1P	RFVGA Input.
25	VCC_VGA1	Power Supply for the RFVGA (3.3 V dc). See Figure 52 for the required components.
26	VCC_VGA1_BALUN	Power Supply for RFVGA Balun(3.3 V dc). See Figure 52 for the required components.
27	VCC_IRM	Power Supply for the Image Reject Mixer (3.3 V dc). See Figure 52 for the required components.
28	IRM_I_P	Positive In-Phase IF Output for the Image Reject Mixer.
29	IRM_I_N	Negative In-Phase IF Output for the Image Reject Mixer.
30	VDD	Power Supply for Logic Circuitry (3.3 V dc). See Figure 52 for the required components.
31	IRM_Q_P	Positive Quadrature IF Output for the Image Reject Mixer.
32	IRM_Q_N	Negative Quadrature IF Output for the Image Reject Mixer.
33	LOP	Local Oscillator Input (Positive). This pin is ac-coupled and matched to 50 Ω.

34	LON	Local Oscillator Input (Negative). This pin is ac-coupled and matched to 50 Ω.
35	SEN	SPI Serial Enable.
36	SCLK	SPI Clock Digital Input.
37	SDI	SPI Serial Data Input.
38	SDO	SPI Serial Data Output.
39	RST	SPI Reset. RESET must be held low (Logic 0) during power on. This is critical for proper programming and reliable operation. Refer to the Theory of Operation section.
40	REF_CLK_P	Filter Calibration Clock.
	EPAD	Exposed Pad. Connect the exposed pad to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

EXTERNAL AGC CONFIGURATION

Lower sideband selected, maximum gain.

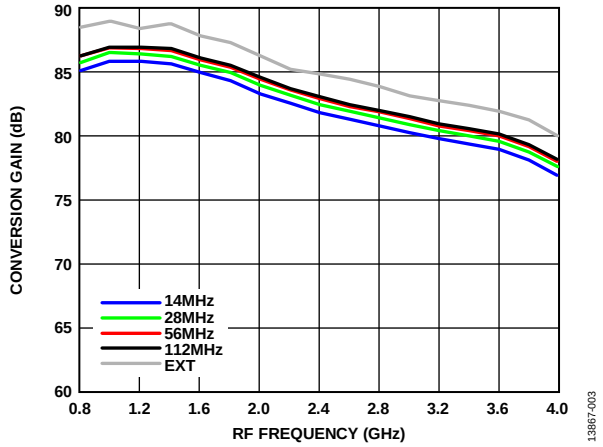


Figure 3. Conversion Gain vs. RF Frequency over Internal and External Filters

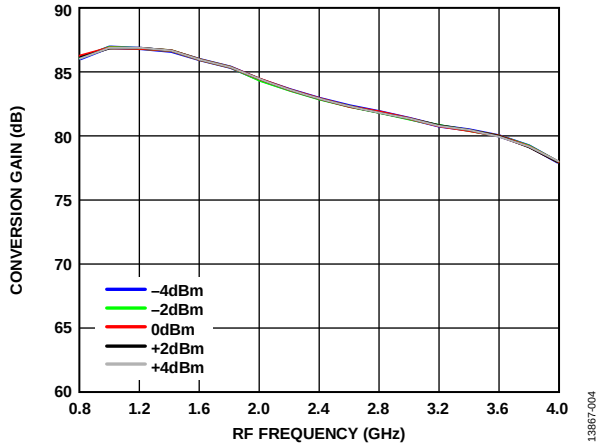


Figure 4. Conversion Gain vs. RF Frequency at Various Local Oscillator (LO) Powers, 56 MHz Filter

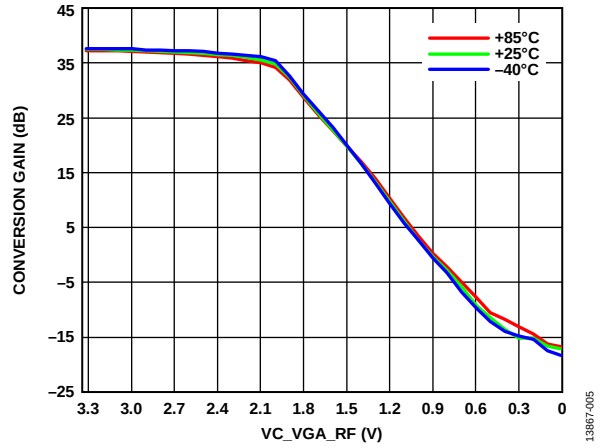


Figure 5. Conversion Gain vs. VC_VGA_RF at RF = 1 GHz, 56 MHz Filter (RF Input Power = −40 dBm, VC_VGA_IF = 0 V)

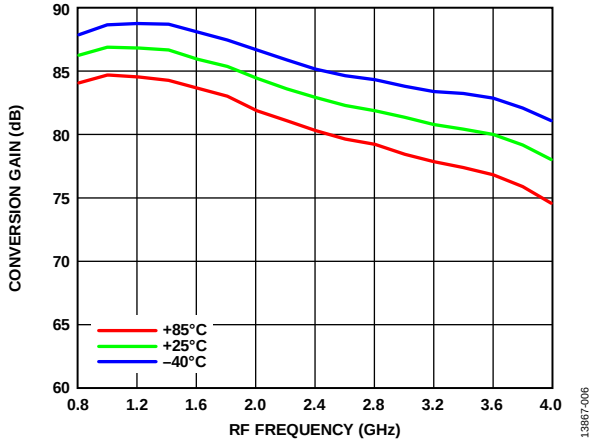


Figure 6. Conversion Gain vs. RF Frequency over Temperature, 56 MHz Filter

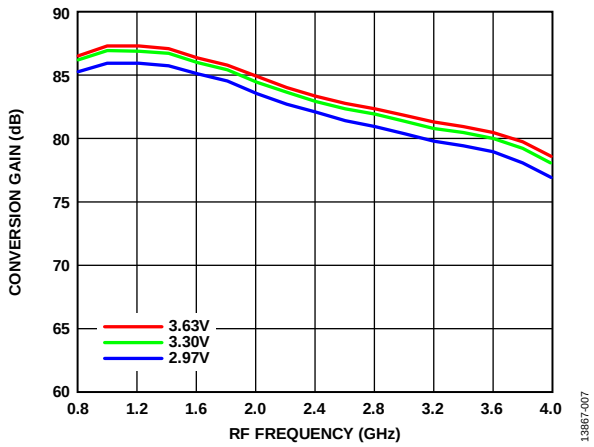


Figure 7. Conversion Gain vs. RF Frequency at Various V_{CCx}, 56 MHz Filter

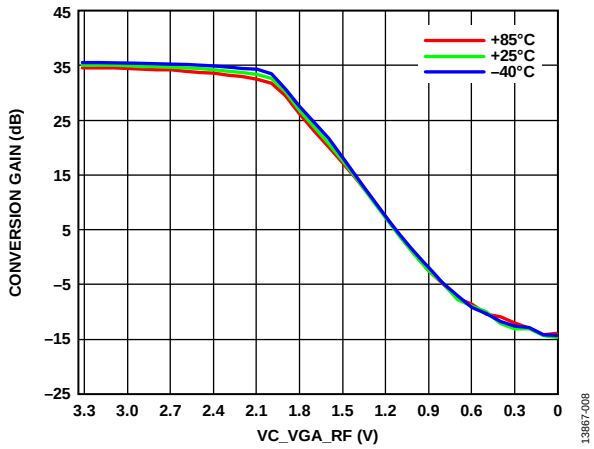


Figure 8. Conversion Gain vs. VC_VGA_RF at RF = 2 GHz, 56 MHz Filter (RF Input Power = −40 dBm, VC_VGA_IF = 0 V)

Lower sideband selected, maximum gain.

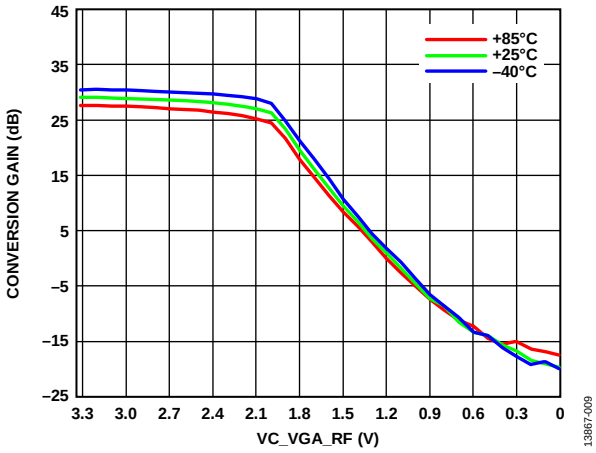


Figure 9. Conversion Gain vs. VC_VGA_RF at RF = 4 GHz, 56 MHz Filter (RF Input Power = –40 dBm, VC_VGA_IF = 0 V)

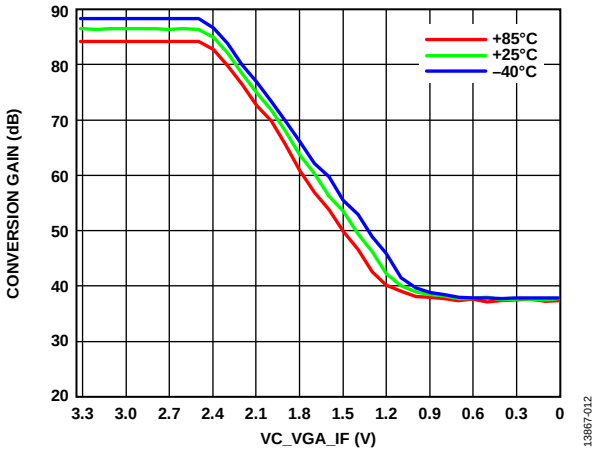


Figure 12. Conversion Gain vs. VC_VGA_IF at RF = 1 GHz, 56 MHz Filter (VC_VGA_RF = 3.3 V)

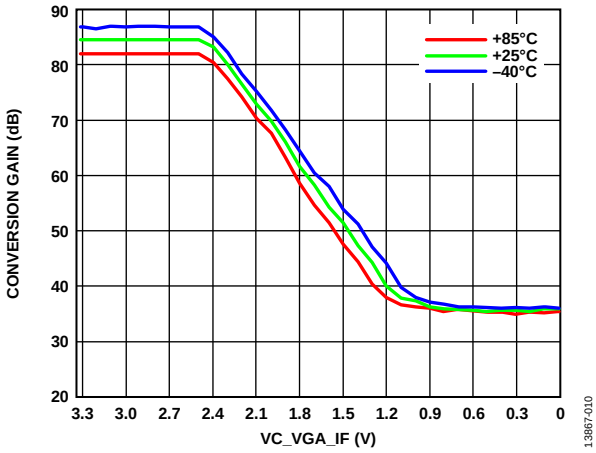


Figure 10. Conversion Gain vs. VC_VGA_IF at RF = 2 GHz, 56 MHz Filter (VC_VGA_RF = 3.3 V)

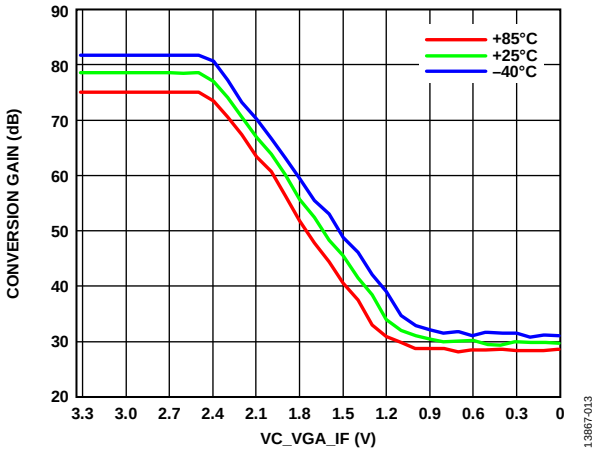


Figure 13. Conversion Gain vs. VC_VGA_IF at RF = 4 GHz, 56 MHz Filter, (VC_VGA_RF = 3.3 V)

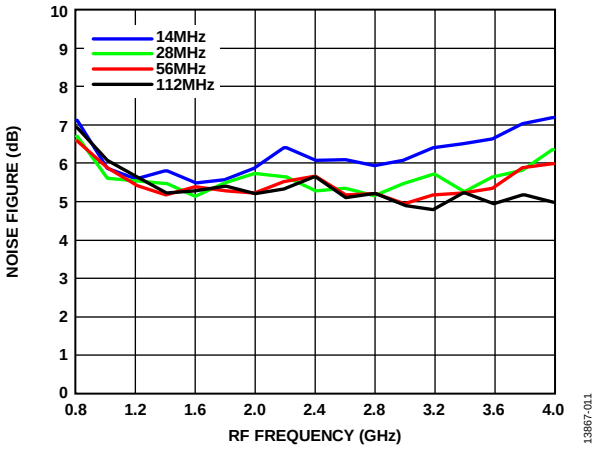


Figure 11. Noise Figure vs. RF Frequency over Internal Filters

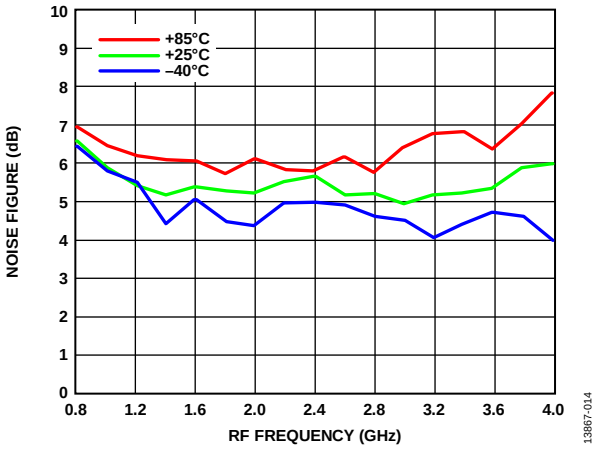


Figure 14. Noise Figure vs. RF Frequency over Temperature, 56 MHz Filter

Lower sideband selected, maximum gain.

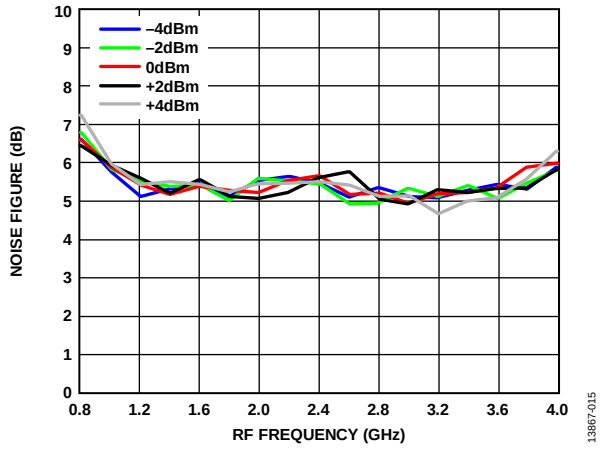


Figure 15. Noise Figure vs. RF Frequency at Various LO Powers, 56 MHz Filter

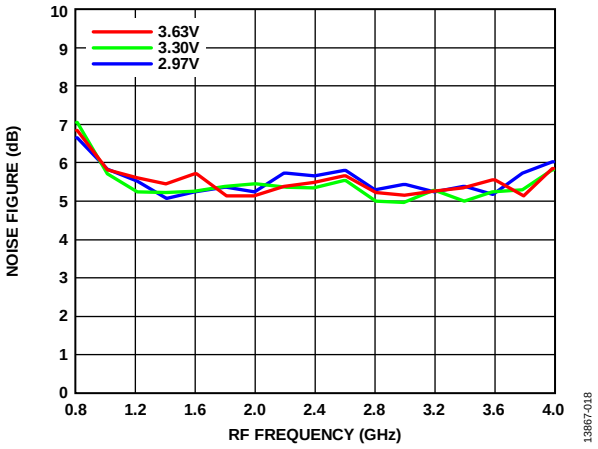


Figure 18. Noise Figure vs. RF Frequency at Various V_{CCx}, 56 MHz Filter

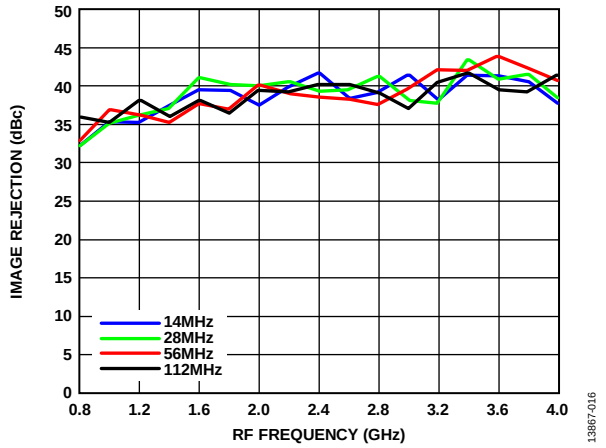


Figure 16. Image Rejection vs. RF Frequency over Internal Filters

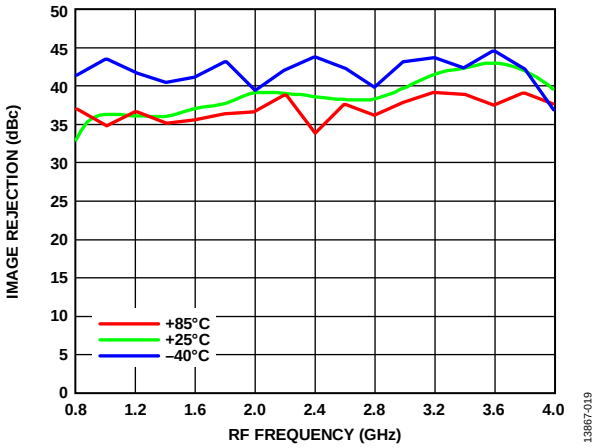


Figure 19. Image Rejection vs. RF Frequency over Temperature, 56 MHz Filter

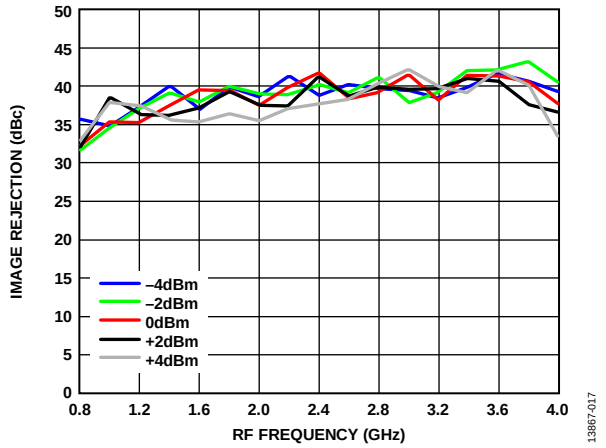


Figure 17. Image Rejection vs. RF Frequency at Various LO Powers, 56 MHz Filter

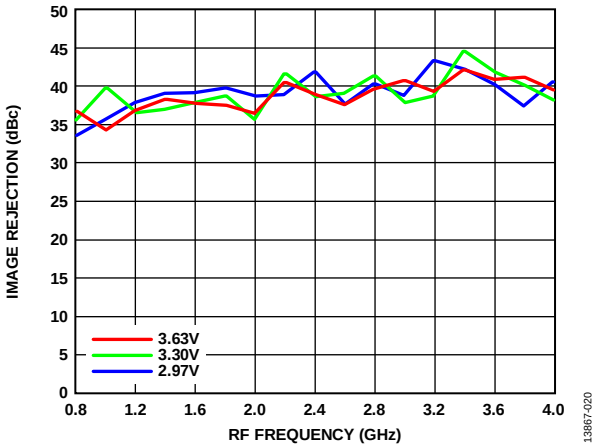


Figure 20. Image vs. RF Frequency at Various V_{CCx}, 56 MHz Filter

Lower sideband selected, maximum gain.

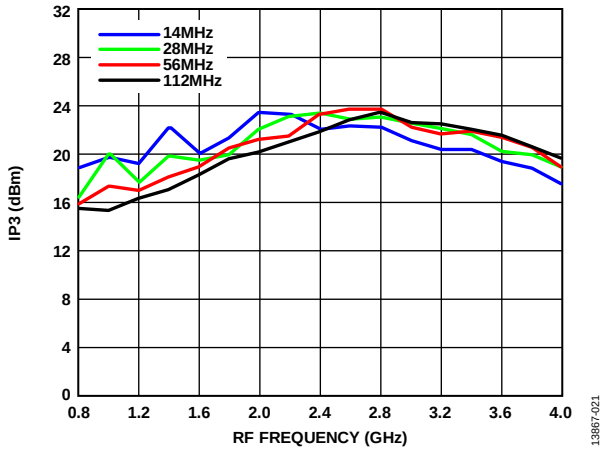


Figure 21. Output IP3 vs. RF Frequency over Internal Filters

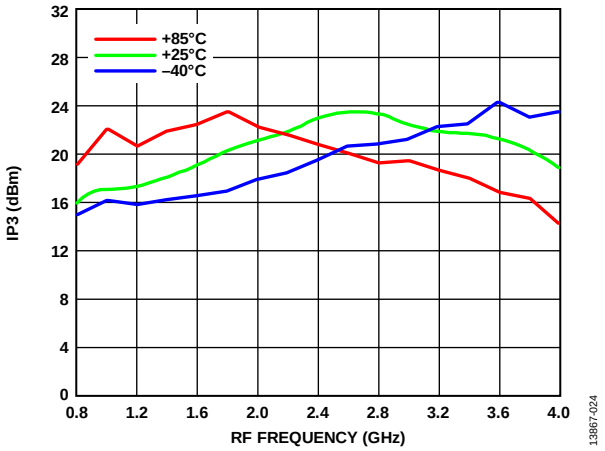


Figure 24. Output IP3 vs. RF Frequency over Temperature, 56 MHz Filter

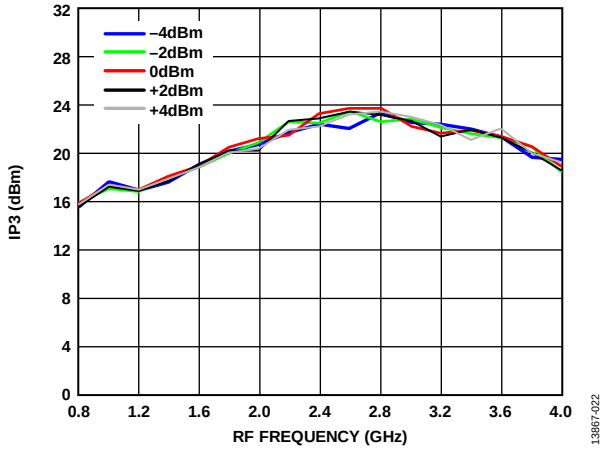


Figure 22. Output IP3 vs. RF Frequency at Various LO Powers, 56 MHz Filter

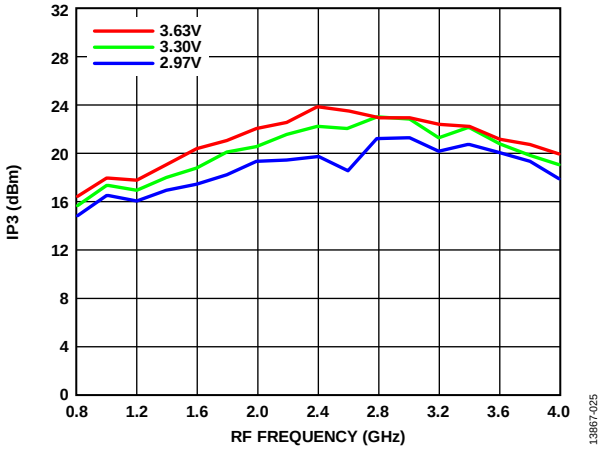


Figure 25. Output IP3 vs. RF Frequency at Various V_{CCx}, 56 MHz Filter

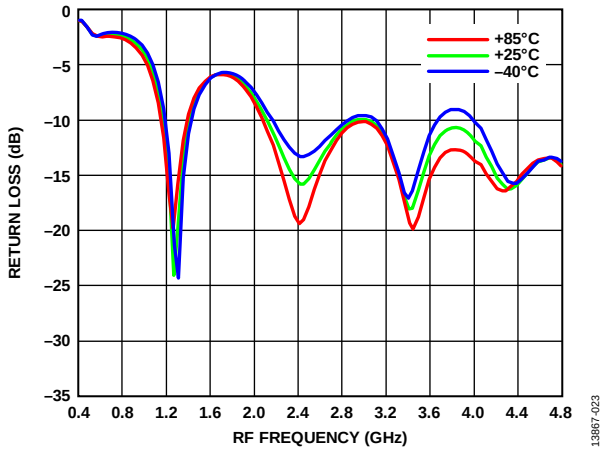


Figure 23. RF Return Loss vs. RF Frequency over Temperature (Optimize RF Return Loss by Adjusting Capacitor C12, see Figure 52)

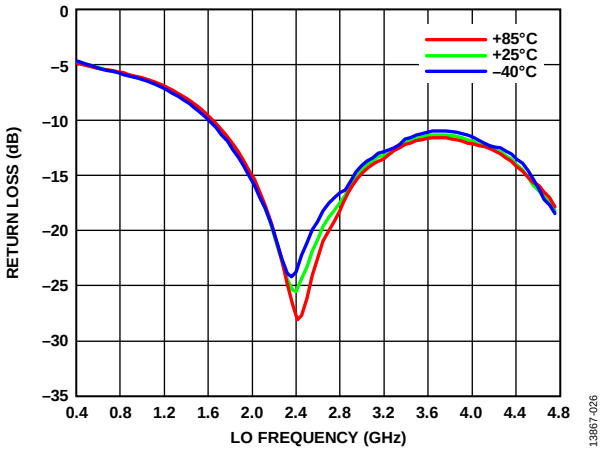


Figure 26. LO Return Loss vs. LO Frequency over Temperature

Lower sideband selected, maximum gain.

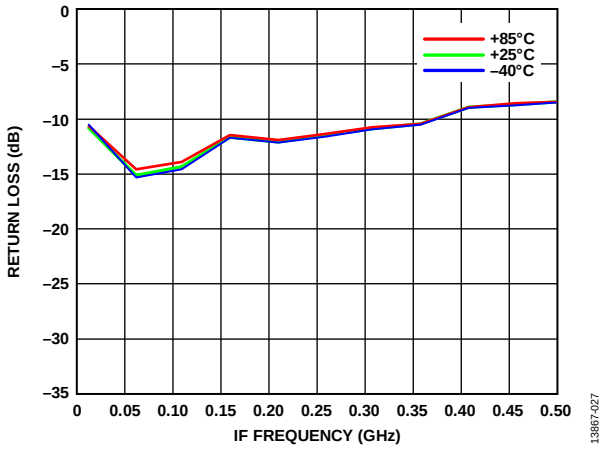


Figure 27. IF Return Loss vs. IF Frequency over Temperature

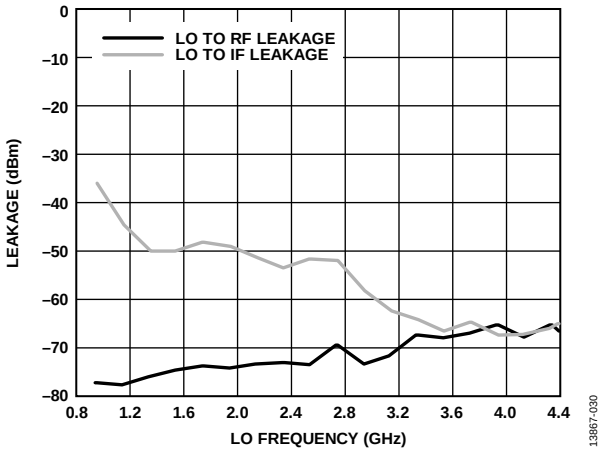


Figure 30. LO Leakage vs. LO Frequency at RF and IF Ports with 56 MHz Filter

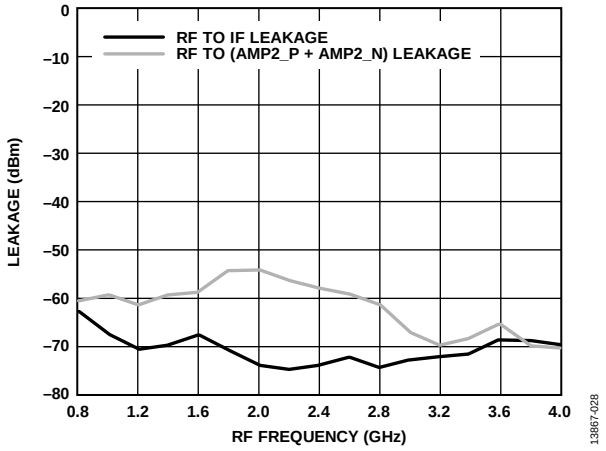


Figure 28. RF Leakage vs. RF Frequency at IF Port with 56 MHz Filter and at (AMP2_P + AMP2_N) Pins

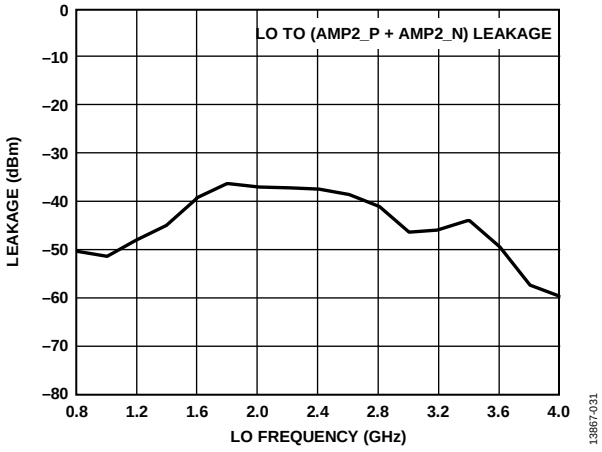


Figure 31. LO Leakage vs. LO Frequency at (AMP2_P + AMP2_N) Pins

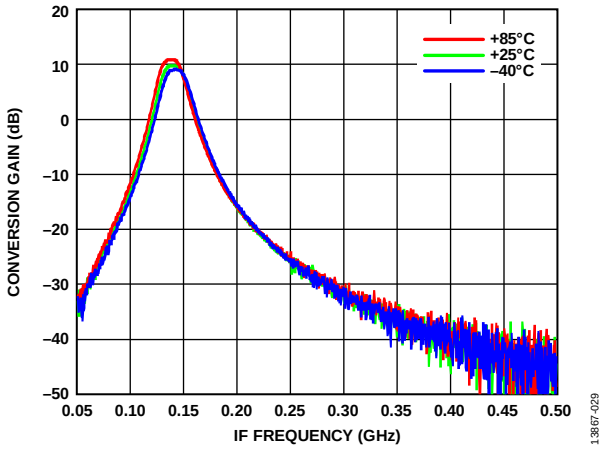


Figure 29. 14 MHz Internal Filter Response vs. IF Frequency at RF = 1 GHz (RF Input Power = −30 dBm, Adjusted VC_VGA_IF and VC_VGA_RF to Achieve 10 dB of Gain)

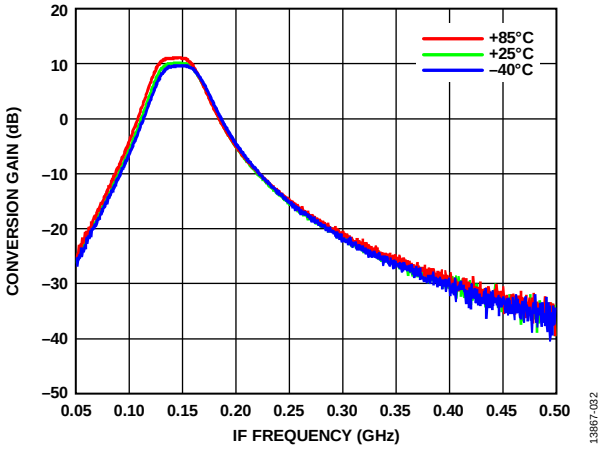


Figure 32. 28 MHz Internal Filter Response vs. IF Frequency at RF = 1 GHz (RF Input Power = −30 dBm, Adjusted VC_VGA_IF and VC_VGA_RF to Achieve 10 dB of Gain)

Lower sideband selected, maximum gain.

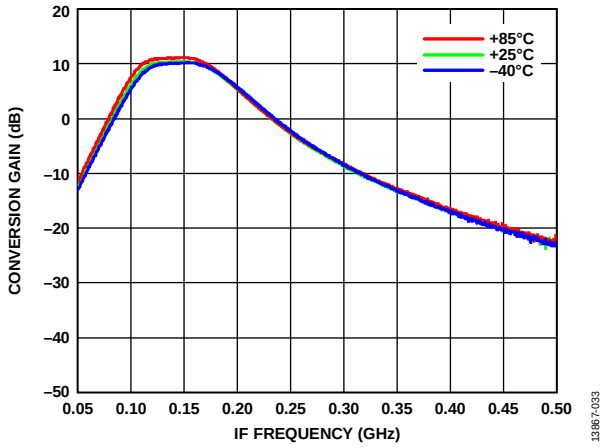


Figure 33. 56 MHz Internal Filter Response vs. IF Frequency at RF = 1 GHz (RF Input Power = −30 dBm, Adjusted VC_VGA_IF and VC_VGA_RF to Achieve 10 dB of Gain)

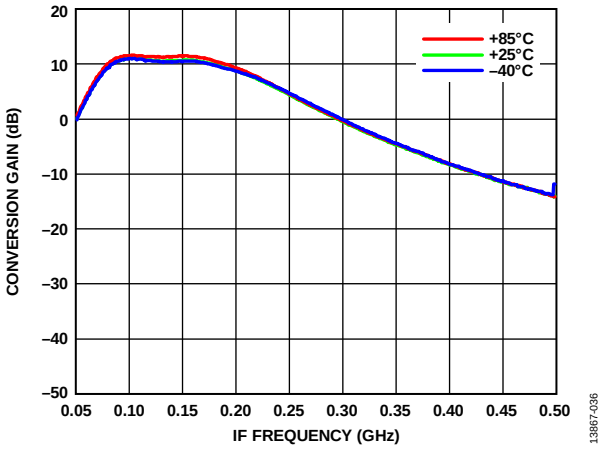


Figure 36. 112 MHz Internal Filter Response vs. IF Frequency at RF = 1 GHz

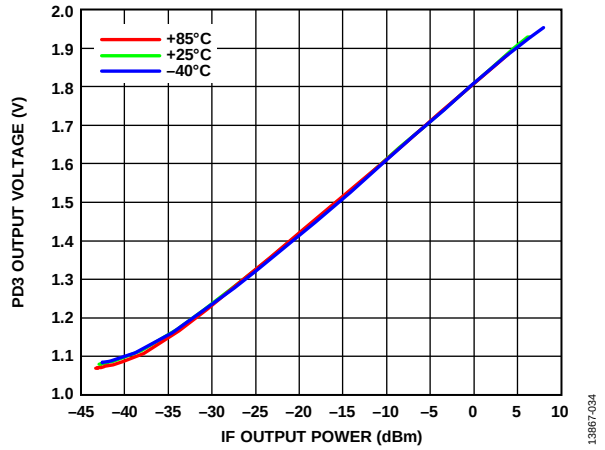


Figure 34. PD3 Output Voltage vs. IF Power Output at RF = 1 GHz, 56 MHz Filter

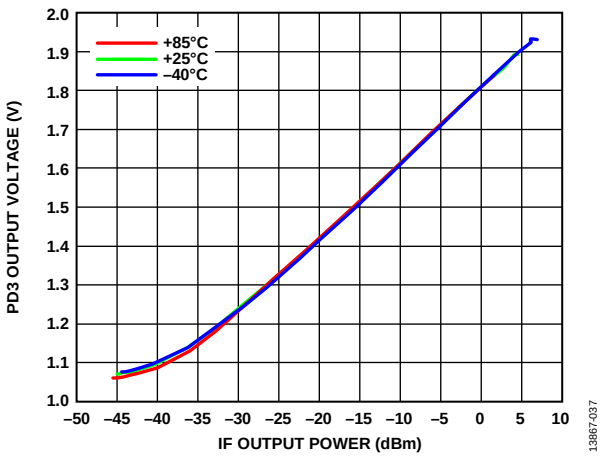


Figure 37. PD3 Output Voltage vs. IF Power Output at RF = 2 GHz, 56 MHz Filter

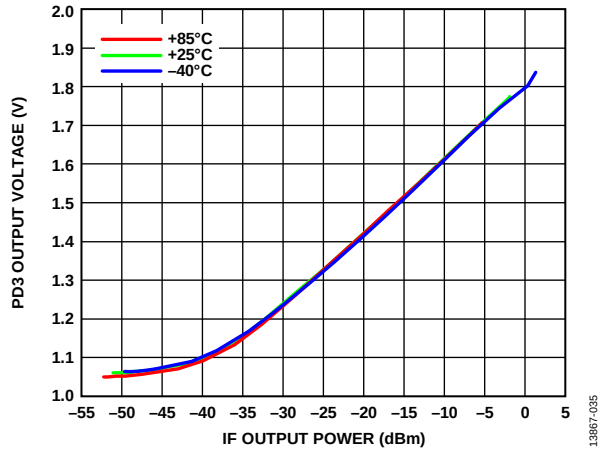


Figure 35. PD3 Output Voltage vs. IF Power Output at RF = 4 GHz, 56 MHz Filter

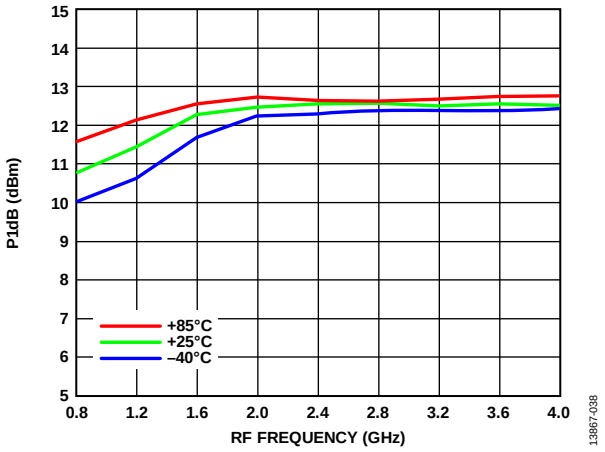


Figure 38. Output P1dB vs. RF Frequency over Temperature, 56 MHz Filter

Lower sideband selected, maximum gain.

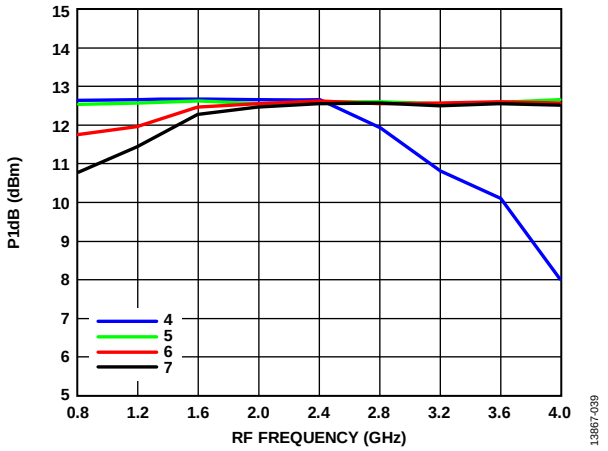


Figure 39. Output P1dB vs. RF Frequency over IF Gain Limit, 56 MHz Filter

INTERNAL AGC CONFIGURATION

P_{OUT} = −9 dBm per tone, lower sideband, and 56 MHz filter selected.

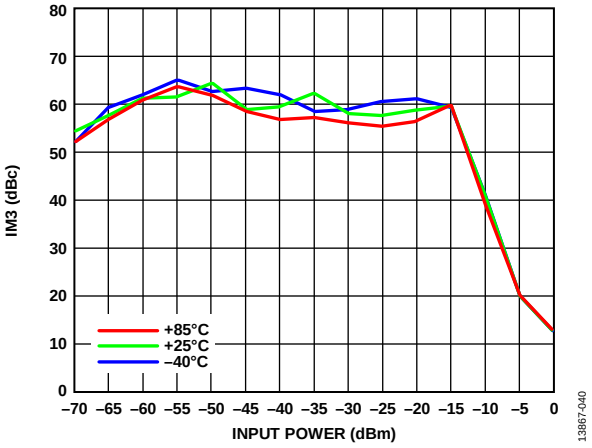


Figure 40. IM3 vs. Input Power over Temperature, RF = 1 GHz

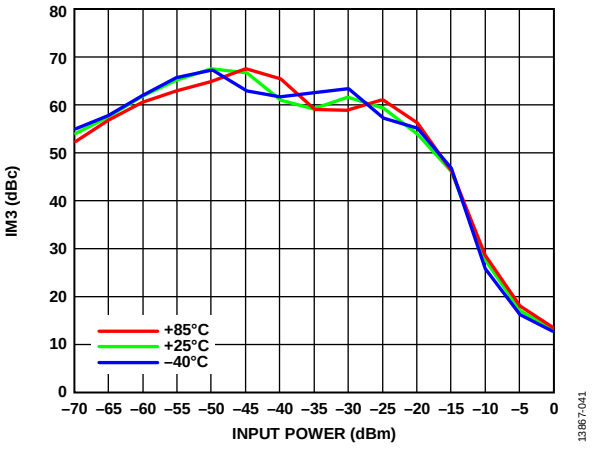


Figure 41. IM3 vs. Input Power over Temperature, RF = 4 GHz

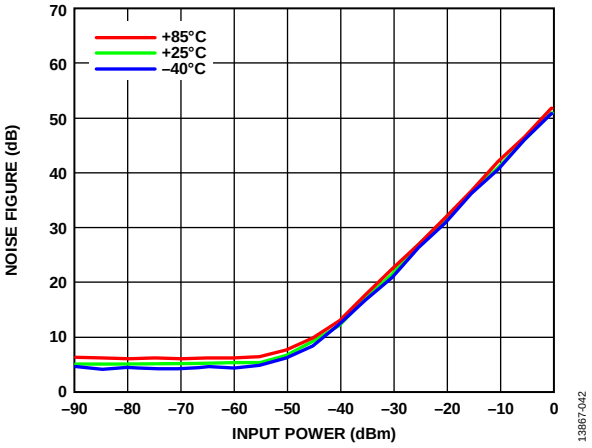


Figure 42. Noise Figure vs. Input Power over Temperature, RF = 2 GHz

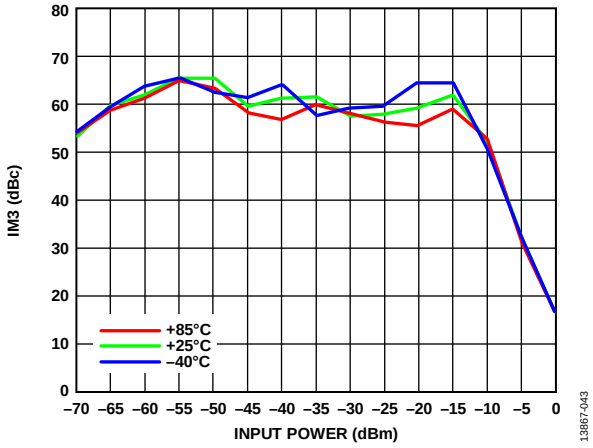


Figure 43. IM3 vs. Input Power over Temperature, RF = 2 GHz

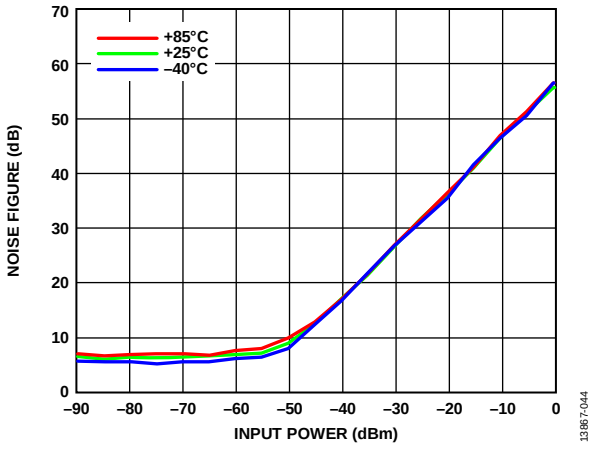


Figure 44. Noise Figure vs. Input Power over Temperature, RF = 1 GHz

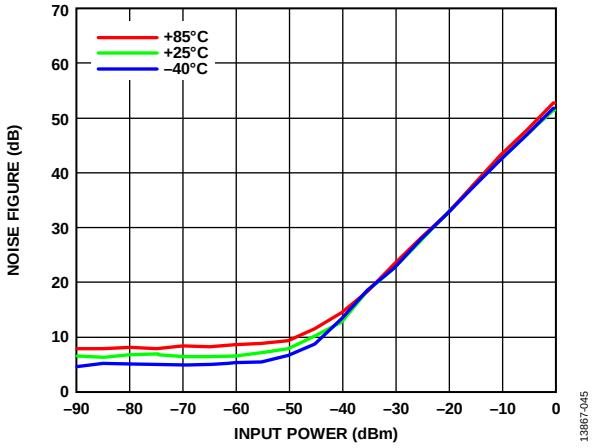


Figure 45. Noise Figure vs. Input Power over Temperature, RF = 4 GHz

P_{OUT} = −9 dBm per tone, lower sideband, and 56 MHz filter selected.

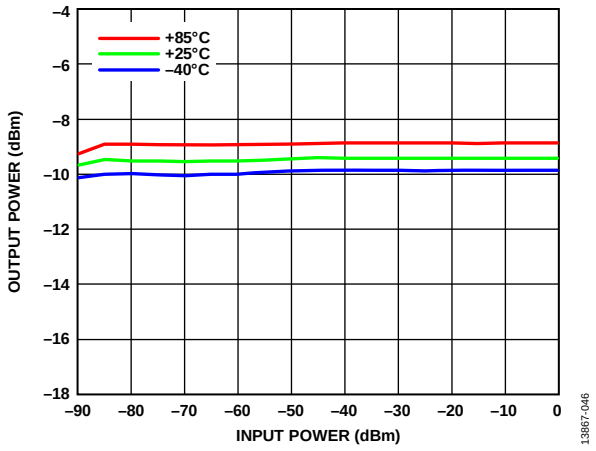


Figure 46. Output Power vs. Input Power over Temperature, RF = 1 GHz

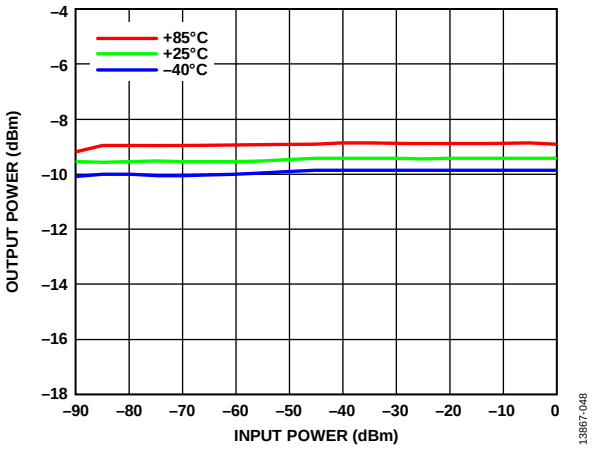


Figure 48. Output Power vs. Input Power over Temperature, RF = 2 GHz

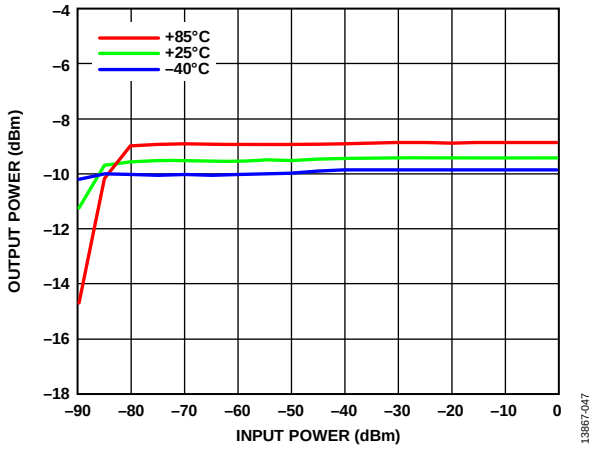


Figure 47. Output Power vs. Input Power over Temperature, RF = 4 GHz

THEORY OF OPERATION

The HMC8100LP6JE is a highly integrated intermediate frequency (IF) receiver chip that converts radio frequency (RF) to a single-ended IF signal at its output. The internal active gain circuit (AGC) of the HMC8100LP6JE is able to actively level the output power at the IF output via SPI control. The gain control of the HMC8100LP6JE can be controlled externally as an alternative option via the VC_VGA_RF and VC_VGA_IF pins with voltages ranging from 3.3 V (minimum attenuation) to 0 V (maximum attenuation).

The HMC8100LP6JE utilizes an input low noise amplifier (LNA) cascaded with a variable gain amplifier (VGA), which can either be controlled by the internal AGC or external voltages, that feeds the RF signals to an image reject mixer. The local oscillator port can either be driven single ended through LON or differentially through the combination of LON and LOP.

The radio frequency is then converted to intermediate frequencies, which can either feed off chip via baseband differential outputs or feed on chip into a programmable band-pass filter. It is recommended during IF mode operation that the baseband outputs be unconnected. The programmable band-pass filter on chip has four programmable bandwidths (14 MHz, 28 MHz, 56MHz, and 112 MHz). The programmable band-pass filter has the capability to adjust the center frequency.

From the factory, a filter calibration is conducted and the center frequency of the filter is set to 140 MHz. This calibration can be recalled via SPI control or the customer can adjust the center frequency, but the calibration value must be stored off chip (see the Register Array Assignments section). An external filter option can be utilized to allow the customer to select other filter bandwidths/responses that are not available on chip. The external filter path coming from the image reject mixer feeds into an amplifier that has differential outputs. The output of the external filter can be fed back into the chip, which is then connected to another amplifier.

A VGA follows immediately after the band-pass filter. Control the IF VGA either by the AGC or external voltages. The output of the variable gain amplifier is the output of the device.

The SPI RESET pin on the HMC8100LP6JE must be held low (Logic 0) during power on. This is critical for proper programming and reliable operation. Apply a RESET low before the bias voltage is applied to the device or use a pull-down resistor on the RESET pin.

REGISTER ARRAY ASSIGNMENTS AND SERIAL INTERFACE

The register arrays for the HMC8100LP6JE are organized into nine registers of 16 bits. Using the serial interface, the arrays are written or read one row at a time, as shown in Figure 50 and Figure 51. Figure 50 shows the sequence of signals on the enable (SEN), CLK, and data (SDI) lines to write one 16-bit array of data to a single register. The enable line goes low, the first of 24 data bits is placed on the data line, and the data is sampled on the rising edge of the clock. The data line should remain stable for at least 2 ns after the rising edge of CLK. The device supports a serial interface running up to 10 MHz, the interface is 3.3 V CMOS logic.

A write operation requires 24 data bits and 24 clock pulses, as shown in Figure 50. The 24 data bits contain the 3-bit chip address, followed by the 5-bit register array number, and finally the 16-bit register data. After the 24th clock pulses of the write operation, the enable line returns high to load the register array on the IC.

A read operation requires 24 data bits and 48 clock pulses, as shown in Figure 51. For every register read operation you must first write to Register 7. The data written should contain the 3-bit chip address, followed by the 5-bit register number for Register 7, and finally the 5-bit number of the register to be read. The remaining 11 bits should be logic zeroes. When the read operation is initiated, the data is available on the data output (SDO) pin. The output data bits are placed on the data line during the rising edge of the clock.

Read Example

If reading Register 2, the following 24 bits should be written to initiate the read operation.

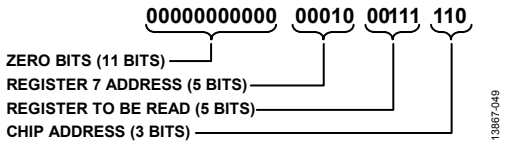


Figure 49. Sample Bits to Initiate Read

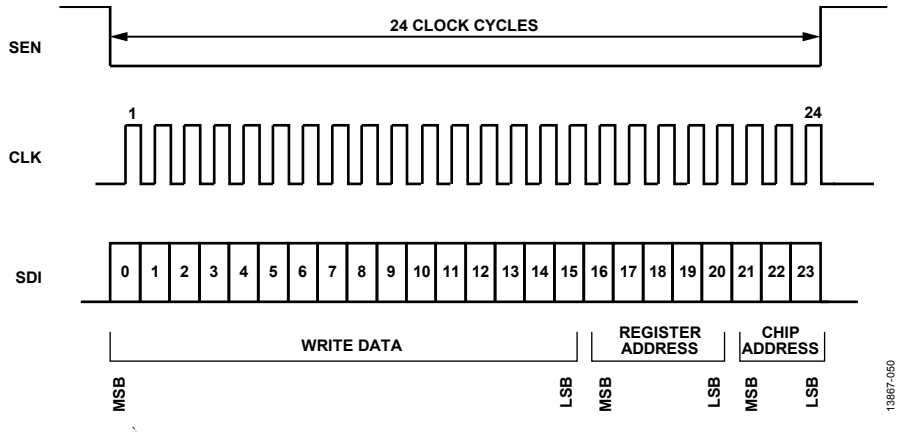


Figure 50. Timing Diagram, SPI Register Write

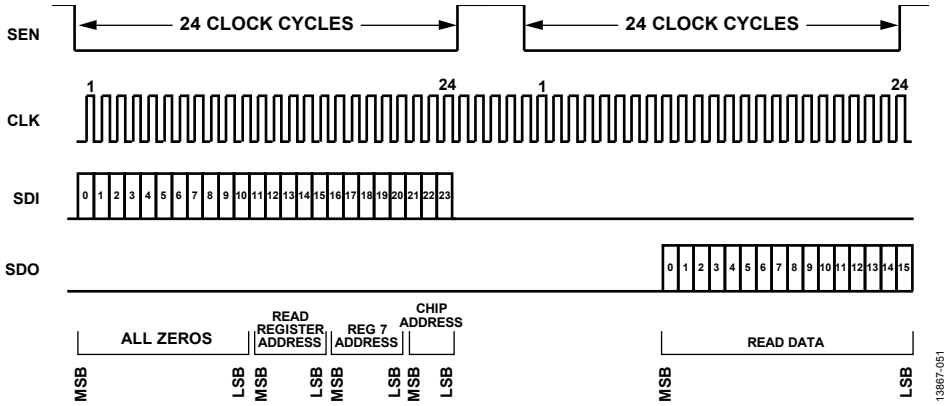


Figure 51. Timing Diagram, SPI Register Read

REGISTER DESCRIPTIONS

REGISTER ARRAY ASSIGNMENTS

In the Access columns (Table 6 through Table 14), R means read, W means write, and R/W means read/write.

Enable Bits

Table 6. Enable Register, (Address 0x01)

Bit No.	Bit Name	Description	Reset	Access
15	PD2_EN	Power Detector 2 enable 0 = disable 1 = enable	0x1	R/W
14	Factory diagnostics	Logic 0 for normal operation	0x0	R/W
13	PD3_AMP1_EN	Auxiliary output (Pin 13) enable 0 = disable 1 = enable	0x1	R/W
12	Reserved	Logic 1 for normal operation	0x1	R/W
11	AMP1_EN	LNA enable 0 = disable 1 = enable	0x1	R/W
10	RF_VGA_EN	RF VGA enable 0 = disable 1 = enable	0x1	R/W
9	IRM_EN	Image reject mixer enable 0 = disable 1 = enable	0x1	R/W
8	FIL2_EN	Filter 2 enable 0 = disable 1 = enable	0x1	R/W
7	IF_VGA_EN	Filter 2 enable 0 = disable 1 = enable	0x1	R/W
6	Factory diagnostics	Logic 0 for normal operation	0x0	R/W
5	PD1_EN	Power Detector 1 enable 0 = disable 1 = enable	0x1	
4	PD3_EN	Power Detector 3 enable 0 = disable 1 = enable	0x1	R/W
3	AGC_EN	Available gain control (AGC) enable 0 = enable 1 = disable	0x1	R/W
2	AMP3_PDWN	Amplifier 3 power-down 0 = enable 1 = disable	0x1	R/W
1	AMP2_PDWN	Amplifier 2 power-down 0 = enable 1 = disable	0x1	R/W
0	IQ_BUF_EN	IQ buffer enable 0 = disable 1 = enable	0x0	R/W

Image Reject and Band-Pass Filter Bits

Table 7. Image Reject and Band-Pass Filter Register, (Address 0x02)

Bit No.	Bit Name	Description	Reset	Access
15	IRM_IS	Image sideband select 0 = lower sideband 1 = upper sideband	0x1	R/W
[14:13]	FIL2_SEL	Internal band-pass filter select 00 = 14 MHz 01 = 28 MHz 10 = 56 MHz 11 = 112 MHz	0x2	R/W
12	SEL_EXT_FIL	Select external filter 0 = internal 1 = external	0x0	R/W
11	Reserved	Not used	0x0	R/W
10	FIL2_CAL_OVR	Override on-chip calibration and use 8-bit word from SPI 0 = use on-chip calibration word 1 = use FIL2_FREQ_SET word from SPI	0x1	R/W
9	FIL2_CAL_EN	Enable filter center frequency calibration 0 = disable 1 = enable (transition from 0 to 1)	0x0	R/W
8	Reserved	Not used	0x1	R/W
[7:0]	FIL2_FREQ_SET	Internal band-pass filter center frequency setting	0x85	R/W

Band-Pass Filter Bits: OTP and SPI

Table 8. Band-Pass Filter Register, (Address 0x03)

Bit No.	Bit Name	Description	Reset	Access
[15:12]	Reserved	Logic 1000 for normal operation	0x8	R/W
11	FIL_OPT_MUX_SEL	Override SPI FIL2_FRQ_SET and use 8-bit word from OTP 0 = select OTP setting 1 = select SPI setting	0x0	R/W
[10:0]	Reserved	Logic 110 1001 1111 for normal operation	0x69F	R/W

AGC

Table 9. AGC Register, (Address 0x04)

Bit No.	Bit Name	Description	Reset	Access
[15:12]	AGC_SELECT	Active gain control (AGC) select 0x3 = internal AGC mode 0xC = external AGC mode	0x3	R/W
11	AGC_EXT_CAP_SEL	Active gain control external capacitor select 0 = no external capacitor 1 = external capacitor	0x0	R/W
[10:8]	AGC_BW	AGC bandwidth 000 = 17 Hz 001 = 22 Hz 010 = 33 Hz 011 = 67 Hz 100 = 83 Hz 101 = 111 Hz (recommended setting) 110 = 167 Hz 111 = 333 Hz	0x4	R/W

Bit No.	Bit Name	Description	Reset	Access
[7:6]	VGA3_GAIN	VGA 3 attentuation 00 = 0 dB (recommended setting) 01 = 5 dB 10 = 10 dB 11 = 15 dB	0x0	R/W
[5:0]	POUT_CTRL	Power output control 0x0 = −54 dBm 0x1 = −53 dBm 0x2 = … 0x3E = +8 dBm 0x3F = +9 dBm	0x30	R/W

AGC: IF Gain Limit Bits

Table 10. AGC Register, (Address 0x05)

Bit No.	Bit Name	Description	Reset	Access
[15:12]	Reserved	Not used	0xA	R/W
[11:9]	IF_GAIN_LIMIT	IF gain limit 000 = 0 dB 001 = 6 dB 010 = 12 dB 011 = 18 dB 100 = 24 dB 101 = 30 dB 110 = 36 dB 111 = 42 dB	0x4	R/W
[8:0]	Reserved	Logic 1 0000 0100 for normal operation	0x104	R/W

Band-Pass Filter Bits: Calibration and 8-Bit Word Frequency

Table 11. Band-Pass Filter Register, (Address 0x06)

Bit No.	Bit Name	Description	Reset	Access
[15:10]	Reserved	Not used	0x0	R
9	FIL2_CAL_OVFL	FIL2 calibration overflow signal	0x1	R
8	FIL2_VCAL_END	FIL2 calibration end signal	0x1	R
[7:0]	FL2_FC_CAL	FIL2 8-bit word frequency setting, read only	0x85	R

AGC: Blocker Power Detector Bits

Table 12. AGC Register, (Address 0x12)

Bit No.	Bit Name	Description	Reset	Access
[15:8]	Reserved	Not used	0xF0	R/W
7	Reserved	Not used	0x0	R/W
6	AGC_BLOCKER_MODE_EN	AGC blocker mode enable 0 = off 1 = on	0x01	R/W
[5:3]	AGC_BLOCKER_PD2_REF	AGC blocker power detector reference level 000 = −4 dBm 001 = −2 dBm 010 = 0 dBm 011 = 2 dBm 100 = 4 dBm	0x3	R/W
		101 = 6 dBm 110 = 8 dBm 111 = 10 dBm		
[2:0]	AGC_BLOCKER_PD2_LOOP_BW	AGC blocker power detector loop bandwidth control 000 = 17 Hz 001 = 22 Hz 010 = 33 Hz 011 = 67 Hz 100 = 83 Hz 101 = 111 Hz 110 = 167 Hz 111 = 333 Hz	0x4	R/W

Phase I Bits

Table 13. Phase I Register, (Address 0x14)

Bit No.	Bit Name	Description	Reset	Access
[15:12]	Reserved	Not used	0xF	R/W
[11:9]	Reserved	Not used	0x0	R/W
[8:0]	I_PHASE_ADJ	I phase adjust	0x0	R/W

Phase Q Bits

Table 14. Phase Q Register, (Address 0x15)

Bit No.	Bit Name	Description	Reset	Access
[15:12]	Reserved	Not used	0xF	R/W
[11:9]	Reserved	Not used	0x0	R/W
[8:0]	Q_PHASE_ADJ	Q phase adjust	0x0	R/W

APPLICATIONS INFORMATION

During operation at P1dB, the IF gain limit of the HMC8100LP6JE, as described in the Register Array Assignments and Serial Interface section, needs to be limited by the radio frequency (RF), as listed in Table 15. There is a recommended IF gain limit setting and maximum allowed IF gain limit setting that is to be used.

SCHEMATIC/TYPICAL APPLICATION CIRCUIT

Table 15. Recommended IF Gain Limit Settings by RF Frequency

RF Frequency (GHz)	Maximum Setting	Recommended Setting
0.8 to 1.8	5	4
1.8 to 2.8	6	5
2.8 to 4.0	7	6

EVALUATION PRINTED CIRCUIT BOARD (PCB)

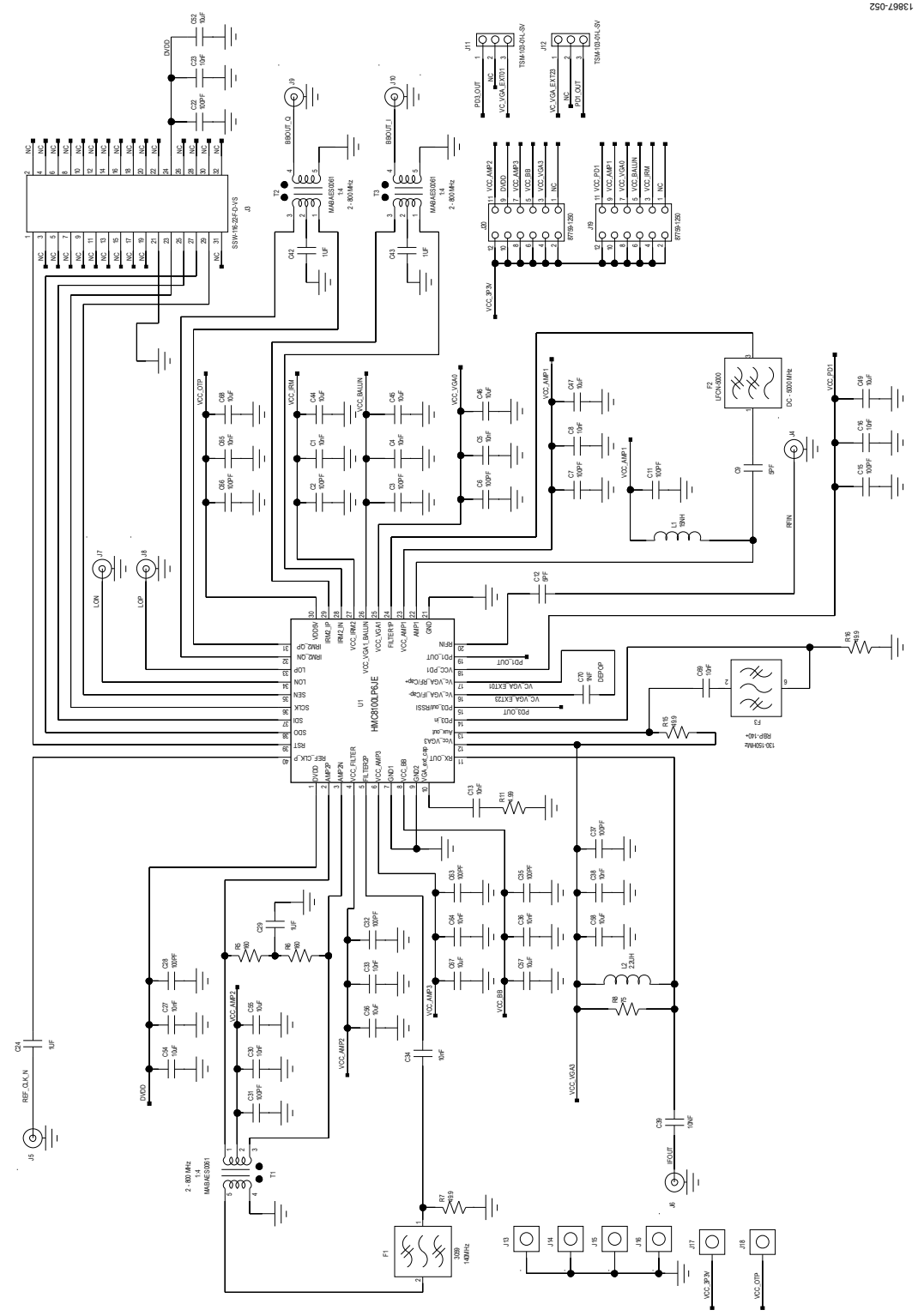


Figure 52. PCB Schematic/Typical Applications Circuit

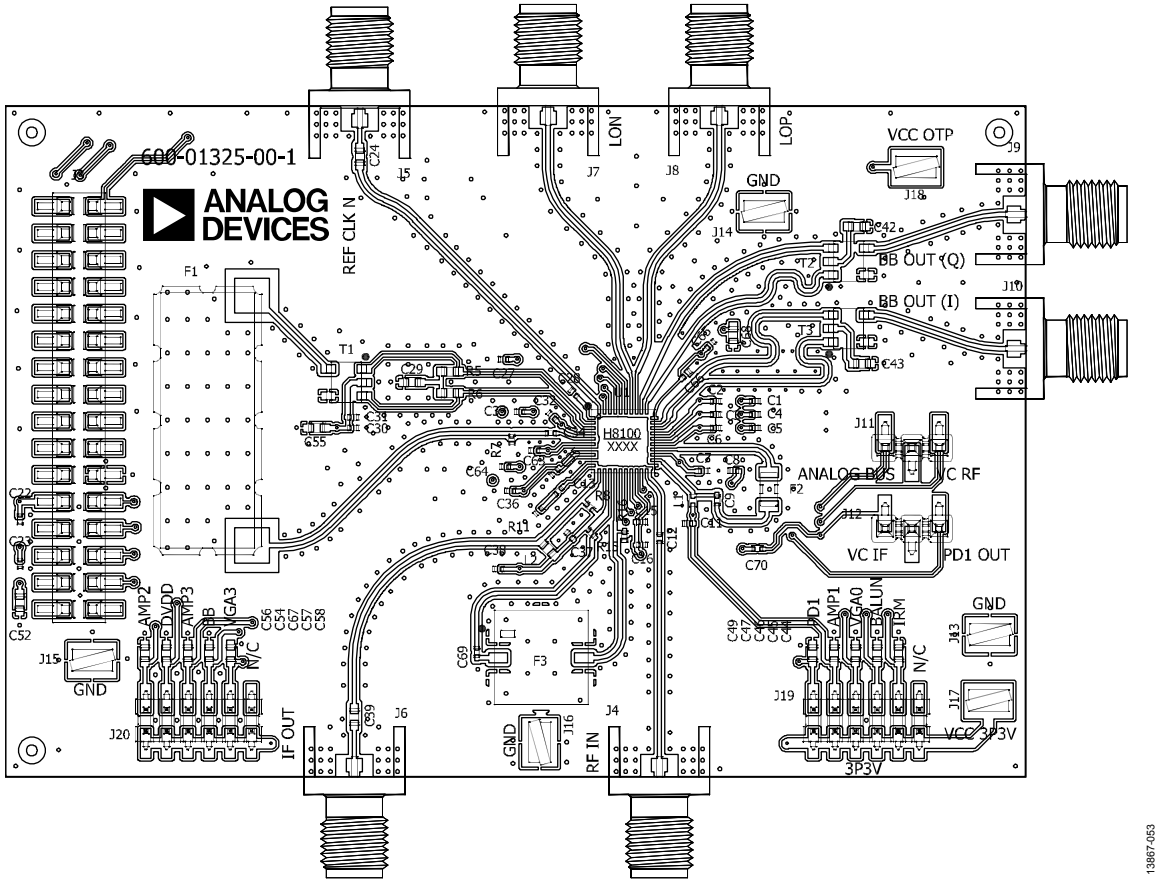
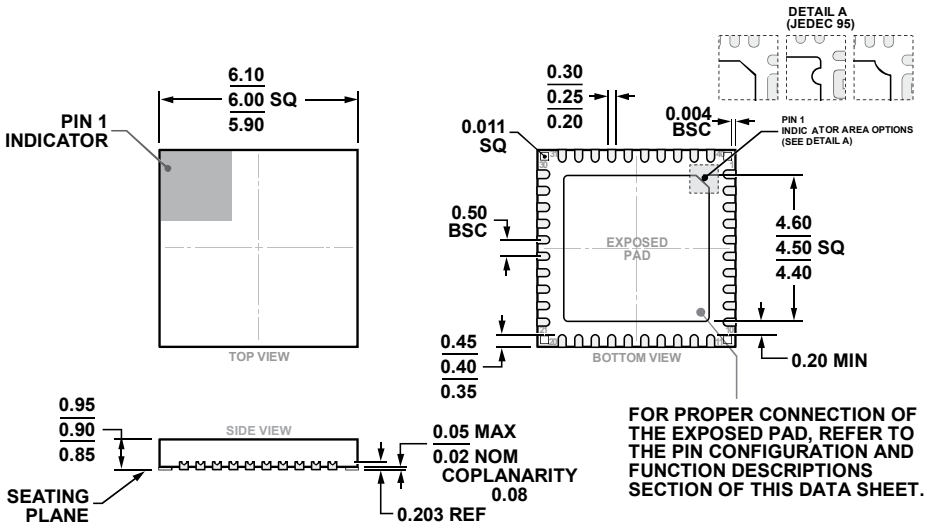


Figure 53. Evaluation PCB

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5.

Figure 54. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.90 mm Package Height
(CP-40-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	MSL Rating[3]	Package Description	Package Option	Package Marking[4]
HMC8100LP6JE	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-22	H8100 XXXX
HMC8100LP6JETR	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-22	H8100 XXXX
EK1HMC8100LP6J			Evaluation Kit		

[1] All models are RoHS compliant.
[2] The HMC8100LP6JE and HMC8100LP6JETR lead finishes are NiPdAu.
[3] See the Absolute Maximum Ratings section.
[4] XXXX is the 4-digit lot number.